PREFERRED RELIABILITY PRACTICES

DESIGN CHECKLISTS FOR MICROCIRCUITS

Guideline:

This guideline provides checklists taken from Government-Industry Data Exchange Program (GIDEP) files to be used as a measure to avoid commonly experienced problems in transistor-to-transistor logic (TTL), complementary-metal-oxide-semiconductor (CMOS), and memory circuit design applications.

Benefit:

Use of this guideline will ensure continued improvement with the use of microcircuits in circuit designs by incorporating data from previously experienced problems into a design checklist. This will apply the experience base from the past and thus provide improved reliability for future space programs.

Center to Contact for More Information:

Johnson Space Center (JSC)

Implementation Method:

See attached Checklists

Technical Rationale:

Information gathered from a history base of known problem areas is presented in easy-to-use checklist form to be used by designers, etc. The checklists are separated into three categories, based on device technology (TTL, CMOS and memory). The guideline can then be used as a reference to avoid incorrect utilization of these component types in circuit design applications which may result in potentially poor reliability.

Impact of Nonpractice:

In many situations, new circuit designs may not adequately incorporate all the relevant past history from a wide data base of previous experience, and hence will not achieve the best possible performance and reliability.

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Related Guidelines:

None

Reference Documents:

MIL-M-38510	Microcircuits, General Specification for
Mil-STD-975	NASA Standard Parts List
MIL-STD-978	NASA Parts Applications Handbook
MIL-STD-1547	Electronic Parts, Materials and Processes for Space and Launch Vehicles
MIL-STD-1562	Lists of Standard Microcircuits

DESIGN CHECKLISTS FOR MICROCIRCUITS

TTL DESIGN CHECKLIST		
1	Only gates from the same package should be connected in parallel.	
2	Take note not to exceed fan-out limit (maximum number of circuits fed input signals from a single output terminal).	
3	Check pin compatibility when using devices from different families or manufacturers.	
4	Check manufacturer interchangeability for minor functional differences.	
5	Maintain equal loading in ac and dc terms on multiple output devices with internal feedback.	
6	The dynamic threshold of low-power schottky (LS) gates varies between 1.1 V and 1.4 V depending on circuit configuration; therefore, slow rise times (greater than 50 nanoseconds) will possibly cause pattern sensitivity.	
7	Gates with outputs driving transmission lines should be situated close to the board periphery.	
8	Consider full-range temperature effects on switching characteristics relative to design application.	
9	Use pull-up resistors on devices with open collector gates.	
10	Consider the frequency dependency of power dissipation when the operating frequency is greater than 1 to 2 MHz.	
11	If decoded outputs from counters, particularly from ripple counters, are being used as clocks to drive counters or memory devices, the decoded outputs of interest should be examined for multiple pulses at counter transitions that might ambiguously operate the driven counters or memory devices, and corrective measures should be taken to non-ambiguously operate the driven circuits.	
12	Take note that low-power, low-power Schottky, and Schottky TTL circuits are known to fail when exposed to 5 microjoules or more of electrostatic discharge (ESD) energy.	
13	Consider "current dumping" effects when a multiple input gate is terminated to a single high impedance source such as a 150-ohm line.	
14	All unused input pins should be tied to high- or low-logic levels, depending on the circuit application. When devices approaching their maximum speed for TTL are used, unused inputs should be "commoned" to used inputs rather than tied high; whereas for low-power Schottky devices with diode inputs, the unused ones can be directly connected to V_{CC}.	
15	Provide isolation for test points so that any foreseeable occurrence, such as shorting between, grounding or external excitation at the test points will not disrupt operational use of the circuit being monitored by the test points.	
16	Consider potential problems involving the use of multiple flip-flops controlled by one or more asynchronous output.	
17	Check interfacing parameters (fan-out, loading, and threshold) when using devices from different families.	

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CMOS DESIGN CHECKLIST		
1	Allow for hold-time and setup-time requirements of CMOS flip-flops, registers, and latches. Inputs to CMOS devices must be stable before and remain stable even after the active clock pulse edge.	
2	Take adequate precautions to avoid ESD damage.	
3	Account for possible incompatibilities with similar part numbers from different manufacturers when establishing parts lists.	
4	Investigate the package choice/reliability tradeoff for each design application.	
5	When using single-stage (unbuffered) multiple-input CMOS devices, consider that both dynamic and static performance of these circuits can deteriorate under certain logic conditions to the extent that logic systems display pattern sensitivity.	
6	Protect signal inputs against overvoltage spikes and input currents exceeding ratings, i.e. many CMOS devices have ten milliamperes as the maximum allowable input current. Consider that if the overvoltage spike is greater than the supply voltage, the parasitic PNP or NPN transistors become forward biased and latch-up can occur.	
7	Excessive current through switches results in latching and destructive breakdown; therefore, protective circuitry is essential.	
8	Consider the noise margin when using 5-volt supply levels. CMOS has an order of magnitude less energy noise margin than TTL (approximately 0.4 nanojoules for CMOS and 4.0 nanojoules for standard TTL).	
9	The power supply should switch on by itself first before signal inputs are applied, since damage may occur if the diode between input and V_{DD} is forward biased.	
10	Slowly rising or falling input signals can lead to multiple triggering, particularly if the supply voltage is poorly regulated, and also to higher supply (I_{DD}) currents.	
11	Maximum power dissipation of the device could be exceeded if input rise and fall times are greater than 15 microseconds, (depending on device type) especially using high current drivers with high supply voltages.	

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CMOS DESIGN CHECKLIST		
12	Terminate all unused inputs; a floating input can turn a CMOS device on, causing faulty operation and possible damage, and also uses increased power since both p- and n-transistors are partially conducting.	
13	Ensure that interfacing parameters between CMOS and other logic families are correct, particularly with regard to loading and thresholds.	
14	Keep interconnections short or use terminations, as long interconnections in high speed systems behave like transmission lines, which can cause reflections and ringing.	
15	Do not use CMOS gates as linear amplifiers; this can destroy buffer gates, cause failure of the device to operate below 4 volts, and make supplier interchangeability even more problematical.	
16	Avoid long, closely spaced, parallel traces on PCB's to minimize crosstalk.	
17	Flip-flops with transmission gate inputs are particularly prone to malfunction if the inputs are driven above and below the supply voltages. This can occur when interfacing from other logic families and from distant boards.	
18	Try not to design to typical values because of the large part-to-part process variations. In many cases guaranteed values are several orders of magnitude larger than typical values.	
19	Reduce ground/power supply inductance (power/ground planes) and use sufficient decoupling capacitors, as simultaneous switching of multiple outputs causes noise and voltage drops on power supplies.	

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MEMORY DESIGN CHECKLIST		
1	Avoid using parts at their maximum supply voltage tolerance and/or at their maximum speed. In a large memory system, noise, loading, and skew problems result in reduced apparent working area and reduced effective speed.	
2	Consider carefully the difficulty in "second sourcing" with memory components, since they are far more complex than standard medium scale integration components (MSI); and very few, if any, have identical replacements.	
3	Avoid mixing several technologies within the same memory system. If this is done great care must be taken to ensure that at no time are the pins of any memory component pulled beyond the component's substrate voltage.	
4	When read-only memories (ROM's) are used to replace wired logic gates, the outputs may show noise or extra transitions, since the ROM is not guaranteed to give a single output transition for a single input transition.	
5	In the use of nichrome fused bipolar programmable read-only memories (PROM's) there has been evidence of fuses growing back after programming and of unblown fuses being subject to decay. Ensure that special freezeout tests and high voltage stressing have been carried out, and also consider the greatly delayed production cycles involved.	
6	Take note when using PROM's that the programming operation on devices from the same family are not necessarily compatible. Examples are the 1602 and 1702 devices in which the programming operation forces "ones" to "zeros," and the 1602A and 1702A devices which force "zeros" to "ones."	
7	Caution must be taken when using common bus lines not to allow more than one device to be enabled at a time. System noise and incorrect data problems could result, and depending on output drive capability, physical damage to the device could occur.	
8	In order to minimize transmission line problems, the driver elements should be located as closely as possible to the memory elements, keeping the connecting printed circuit lines as short as possible.	
9	Asynchronous input signals applied to a ROM should be permitted to change within an access time sufficient to meet setup and hold times, prior to clocking the output register. If this does not occur the contents of the output register may be completely unpredictable.	
10	Periodically check PROM programming electrical specifications, since manufacturers often change their recommended programming method to improve programming yields.	
11	Ensure the correct programming conditions (voltage, duration, etc.) when programming PROM's.	
12	Ensure that shift register drivers have sufficient dumping capabilities, otherwise positive or negative spikes may be coupled from one clock to the opposite phase. Spikes may reach over the substrate voltage and activate parasitic substrated transistors and destroy data.	
13	Memory products usually dissipate power at significantly higher levels per package than most large-scale integration (LSI) and MSI components. It is therefore very important that adequate cooling arrangements be made, because the power dissipation per unit area can approach an order of magnitude greater than ordinary TTL.	

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14	Allow in the design for the ROM/PROM access time differences from various parts of the array. Differences of four to one have been found for various address locations.	
15	Take caution when using dynamic MOS shift registers (SR's) as low-speed power-saving circuits, since data can be lost if the SR clock speed is reduced instantaneously. The lower frequency limit applies only at high ambient temperatures and not at self-heated high-junction temperatures produced at high clock frequencies.	
16	Take note that when using floating gate metal oxide semiconductor (MOS) PROM's, bit loss occurs under x-ray and nuclear radiation. In addition, problems of inadequate erasure due to poorly calibrated ultraviolet sources can arise.	
17	Take caution when using MOS electrically alterable PROM's, since data loss can occur from cells subjected to greater than 10^9 accesses. Given an access time of 1 microsecond, the data could be lost within an hour if continuous reads are made from one location.	
18	Power supply slew characteristics should be evaluated carefully. Two separate problems have been noted. One problem is that at switch-on, a slowly rising power supply may not initialize the random access memory (RAM) logic correctly so that a subsequent initializing procedure is required. Another problem is that sharp, small supply voltage changes that occur in normal memory system operation can cause data loss in some supplier dynamic memory products.	
19	Operating temperatures have to be considered very carefully. Because of their complexity, memory components tend to be more sensitive to temperature extremes than other types of devices.	
20	Consider that large MOS memory systems often require error correction and detection (the inclusion of "Hamming" error correction codes in the design). This approach improves the effective system reliability by two orders of magnitude, and the associated error indicators simplify scheduled maintenance.	
21	Consider access time measurement criteria carefully. While some manufacturers measure access times to the V_{OL} and V_{OH} voltage levels, others measure access to the 1.5 voltage level for both high- and low-level outputs. Additionally, some suppliers specify two output loads in their dc characteristics, but measure access time against one output load.	
22	Many dynamic RAM's require a substrate bias supply (V_{BB}) to ensure correct operation. Unless this bias supply is raised before the main supply and dropped after the main supply, high currents may be drawn. Also, if the bias supply is reversed even in a transient mode, the parasitic substrate transistor will draw extremely high currents. Since the internal capacitances of the RAM are terminated to the substrate, very good transient bypassing is required.	
23	Take care when using bipolar memory devices (e.g., many ROM/PROM devices) with PNP transistor low-power Schottky style inputs. It is important that the inputs not be pulled below ground until the PNP device is saturated; otherwise, very long access times will be observed.	
24	Allow for input/output coupling features of static RAM's in the system design. Although possibly not shown on the write- cycle data published by the manufacturers, the input data may appear on the output during the write mode.	