PREFERRED
RELIABILITY
PRACTICES

THERMAL CYCLING

Practice:

As a minimum, run eight thermal cycles over the approximate temperature range for hardware that cycles in flight over ranges greater than 20^{o}C. The last three thermal cycles should be failure-free.

Benefit:

Demonstrates readiness of the hardware to operate in the intended cyclic environment. Precipitates defects from design or manufacturing processes that could result in flight failures.

Programs That Certified Usage:

ATLAS, CENTAUR, Space Electronic Rocket Tests (SERTs) 1 and 2, Communication Technology Satellite (CTS), GOES, COBE, NOAA, LANDSAT, Solar Maximum Mission

Centers to Contact for Information:

- Lewis Research Center (LeRC)
- Goddard Space Flight Center (GSFC)

Implementation Method:

As part of ATP, run at least eight thermal cycles over the temperature range experienced by the hardware during storage, shipping, launch, flight, and reentry. The maximum and minimum temperatures anticipated should be exceeded by 10^{o}C. The last three thermal cycles should be failure-free.

Equipment must stabilize at these limits before cycling to the opposing limit. Equipment generally should be operated within the anticipated thermal range rather than at the thermal limits.

Thermal cycling should be conducted in a vacuum if the test item is designed to operate in a vacuum.

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Technical Rationale:

Thermal cycle modeling has shown that the general form of the thermal cycling test math model is given by Equation (1).

$$TE = F \times P_d \left[1 - \exp(-\lambda_0 N K^{\Delta \Delta T})\right] \quad (1)$$

Where:
- TE = Test Effectiveness
- F = Fraction of total failures that can be precipitated by a thermal cycle
- P_d = Probability of detection
- λ_0 = Failure rate at T_0
- N = Number of thermal cycles
- K = A constant
- ΔT = $T - T_0$
- T = Operating temperature for λ
- T_0 = Operating temperature for λ_0

Fig. 1 shows that the failures available are the sum of three parts:

1. Failures detected by thermal cycle tests
2. Undetected failures
3. Failures not precipitated

For single temperature range of 50°C, the test effectiveness equation reduces to Equation (2).

$$TE = 0.9 \times P_d \left(1 - e^{-0.0864N}\right) \quad (2)$$

Figure 2 shows a plot of Equation (2) based on a probability of detection, P_d, of 0.9. The equation is based on values of λ_0 and K that were found by solving two simultaneous equations derived from the data base provided in Table 1.

Printed circuit boards (PCBs) are especially prone to solder joint cracking. The design is required to minimize the mechanical forces, as generated by thermal mismatch of materials or vibration, in the solder joints.

THERMAL CYCLING

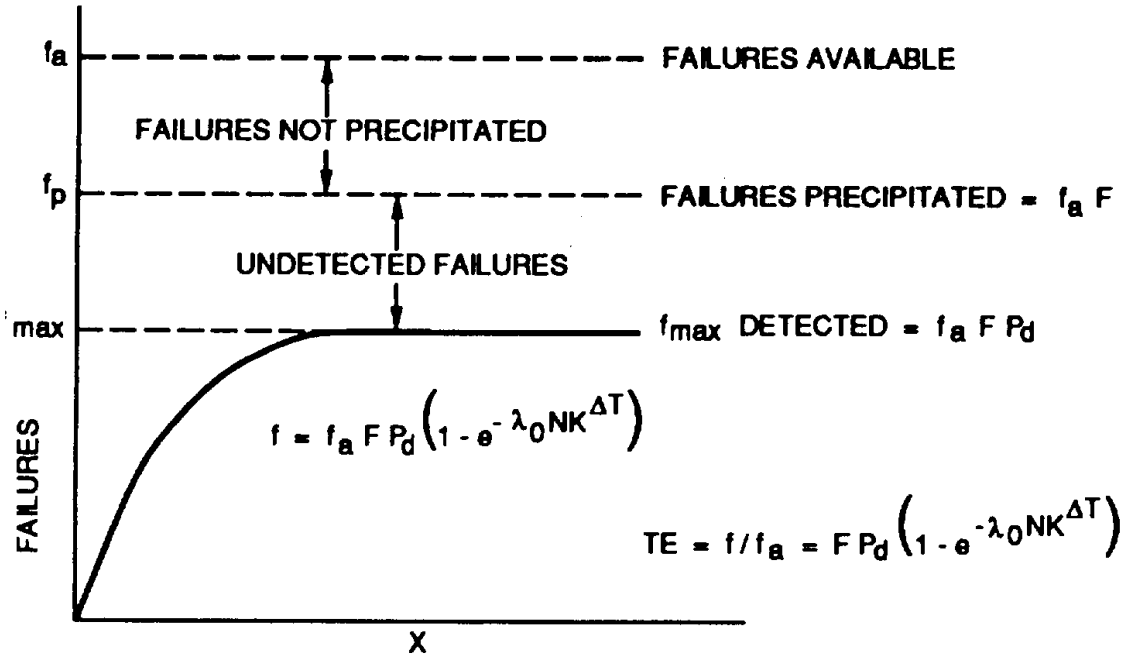

Fig. 1 General Form of TC Test Model

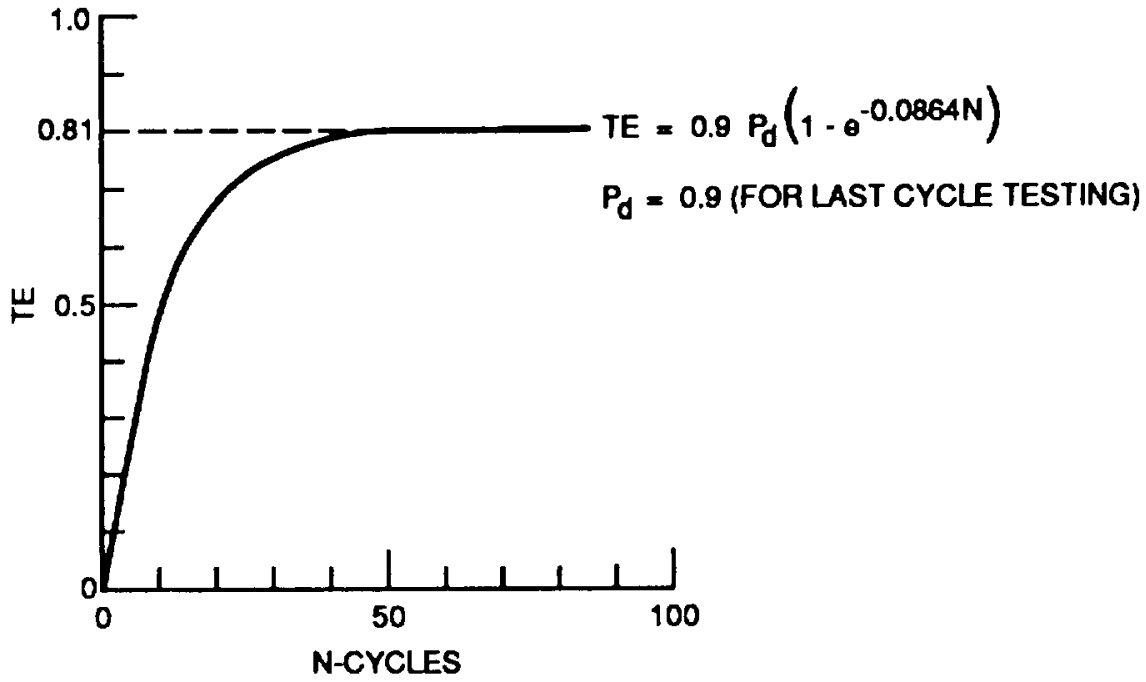

Fig. 2 Test Effectiveness Plot for $\lambda T = 50^0C$

THERMAL CYCLING

Impact of Nonpractice:

Design and manufacturing defects that could have been detected during ground testing manifest themselves during flight.

Related Practices:

Solder Joint Fatigue Cycles, Thermal Dwell Testing.

References

1. GDCD BNZ 69-007, Curssell, G. M., "Atlas and Centaur Component Acceptance Test Plan," 1984.

2. NASA TMX-53731, Van Orden, R. E., "Mounting of Components to Printed Wiring Boards," 1968.

3. Laube, R. B., "Space Vehicle Thermal Cycling Test Parameters," Proceeding of the Institute of Environmental Sciences, 1983.

4. Nelson, C. E., "System Level Reliability Thermal Cycling," Proceeding of the Institute of Environment Sciences, 1983.