PREFERRED RELIABILITY PRACTICES

SPACE RADIATION EFFECTS ON ELECTRONIC COMPONENTS IN LOW-EARTH ORBIT

Practice:

During system design, choose electronic components/devices which will provide maximum failure tolerance from Space Radiation Effects. The information below provides guidance in selection of radiation hardened (rad-hard) solid state devices and microcircuits for use in space vehicles which operate in low-earth orbits.

Benefit:

This practice provides enhanced reliability and availability as well as improved chances for mission success. Failure rates due to space radiation effects will be significantly lower, and thus system down time will be much lower, saving program cost and resources.

Programs That Certified Usage:

Space Shuttle Orbiter

Center to Contact for More Information:

Johnson Space Center (JSC).

Implementation Method:

Space Radiation Environment, Essential Basics: Radiation in Space is generated by particles emitted from a variety of sources both within and beyond our solar system. Radiation effects from these particles can not only cause degradation, but can also cause failure of the electronic and electrical systems in space vehicles or satellites. Even high altitude commercial airliners flying polar routes have shown documented cases of avionics malfunctions due to radiation events.

Primary Cosmic rays interact with gaseous and other matter at high altitudes and produce secondary radiation. The combination of both contributes to the Space Radiation environment. The fusion process on the Sun's interior produces electrons and protons in great abundance along with helium and other heavier nuclei, which travel towards earth as the solar wind. This solar wind radiates out from the sun in all directions; but the flux of these particles varies with sunspot activity and solar flares. In addition to the particles originating from the sun are particles from other stars and heavy ion sources such as novas and supernovas in our galaxy and beyond. In interplanetary space these ionizing particles constitute the major radiation threat. These particles are influenced by planetary or earth's magnetic field to form radiation belts, which in earth's case are known as Van Allen Radiation belts, containing trapped electrons in the outer belt and protons in the

inner belt. The composition and intensity of the radiation varies significantly with the trajectory of a space vehicle.

Experience with many spacecraft since Explorer I shows that higher electron concentrations are observed between 45 degrees and 85 degrees latitude in both the northern and southern hemispheres, indicating that the belts descend to a lower altitude in these regions. For low inclination orbits, less than 30 degrees, the electron concentrations are relatively low. Due to the earth's asymmetric magnetic field, a region in the Atlantic near Argentina and Brazil, known as South Atlantic Anomaly (SAA), has relatively high concentrations of electrons. The SAA is known to cause problems such as: single event upsets (SEU) in altimeter electronics gate arrays, and "hard" SEU's in the Space Shuttle Orbiter's Star Tracker's Analog-to-Digital converter. The March 1991 solar storms significantly increased the charged particle distributions in the Van Allen belts, also creating a third belt.

In addition to the trapped charged particles in Van Allen radiation belts (electrons and protons), the spacecraft experience radiation threats from high energy heavy ions in space called Galactic Cosmic rays, and secondary X-Rays or Bremstrahlung generated by particles penetrating the skin of the space-craft while they lose energy. This type of electromagnetic radiation is a significant percentage of the total component producing total dose effects. The usual (Centimeter Gram Second) unit used to specify radiation dose or deposited energy is the "rad," which is defined as 100 ergs/gm of material. The material is always specified in parentheses, e.g., rad(Si). But the International system of units (SI) defines an essentially Meter Kilogram Second (MKS) units for absorbed dose called the "gray" (GY). One GY is defined as the deposition of 1 joule per kilogram of radiation energy, i.e 1GY = 100 rads.

Solar Flares also contribute varying quantities of electrons, protons, and lower energy heavy ions. Solar flares occur randomly at different times, and during times of high solar activity may contribute very high fluxes of particles over periods of hours or days. Heavy ions of various energies cause single event effects (SEE). A convenient way to express the transient charge generated by these heavy ions or charged particles is in charge per unit length, e.g. pC/micron. However a more frequently used term (but less intuitive) to express the same thing is called, "Linear Energy Transfer or LET", which is expressed in MeV.cm^2/mg.

In bit-storage devices the high energy heavy-ions cause bits to change, and are expressed in terms of bit error rates or SEU Error Probability. The SEU Error Probability is a number generated by computer from three data inputs: (a) the expected distribution of particles vs. LET, (b) the device cross-section for upset or latch up as function of LET, usually obtained from laboratory measurements, and (c) a calculation of expected error rate that combines the first two relationships with a calculation of the effect of the omni-directional particle flux on the charge produced in the device by the incident particles. Computer programs are available that perform this calculation. The net result is a fixed number for the upset or latch up probability. The following rules must be observed for estimating total dose environments:

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Criteria for Selection of Parts for Enhanced Reliability:

a) For Space vehicles or satellites in low inclination (≤ 28 degrees) Low Earth Orbit ((LEO), < 500 km or 270 nmi) in both northern and southern hemispheres, typical dose rates due to trapped Van Allen electrons and protons are 100-1000 rad(Si)/year.
b) For Space vehicles or satellites in higher inclinations ($20 < I \geq 85$ degrees) LEO in both northern and southern hemispheres, typical dose rates due to increased number of trapped electrons are 1000-10,000 rad(Si)/year.

There are three categories of components having the following characteristics:

(1) Commercial:
* Process and Design limit the radiation hardness
* No lot radiation controls
* Hardness levels:
  Total Dose: 2 to 10 krad (typical)
  SEU Threshold LET: 5 Mev/mg/cm^2
  SEU Error Rate: 10E-5 errors/bit-day (typical)
* Customer performs rad testing, and assumes all risk
* Customer evaluation and risk

(2) Rad Tolerant:
* Design assures rad hardness up to a certain level
* No lot radiation controls
* Hardness levels:
  Total Dose: 20 to 50 krad (typical)
  SEU Threshold LET: 20 MeV/mg/cm^2
  SEU Error Rate: 10^{-7} - 10^{-8} errors/bit-day
* Usually tested for functional fail only, risky
* Customer evaluation and risk

(3) Rad Hard:
* Designed and processed for particular hardness level
* Wafer lot radiation tested
* Hardness levels:
  Total Dose: > 200 krad to >1 Mrad
  SEU Threshold LET: 80-150 MeV/mg/cm^2
  SEU Error Rate: 10^{-10} to 10^{-12} errors/bit-day
* Latch up:
  None present in Silicon-on-Insulator/Silicon on Sapphire (SOI/SOS)
  Complimentary Metal Oxide Semiconductor (CMOS)-technologies
  Exhibit Low SEU sensitivity for SEE's

NOTE: Although Class S does not guarantee that the parts are rad-hard, the design process does dictate whether a part is rad-tolerant or not.

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Using rad-soft components does not significantly reduce cost, but greatly increases risk. There are no components that are ideal for all parameters. IC design requires many tradeoffs in performance (cost included as performance parameter). Commercial components are useful only for commercial applications, where low cost, latest technology (even if it is immature), and high speed takes precedence over extreme temperatures and voltage ranges. Shielding these devices in Space Applications is a futile effort, especially for Single Event Effects such as SEU and Single Event Latch up (SEL).

Total Dose Hardness Levels of Various Technologies : It should be noted that Bipolar device operation depends upon minority carrier current levels flowing through the substrate, while Metal Oxide Semiconductor (MOS) technologies operate upon majority carrier current flows at the surface of the substrate. (Junction Field Effect Transistors depend upon majority carrier currents through the substrate). This is what makes their interaction with radiation different . Table 1 shows a comparison of Bipolar to MOS devices and radiation hardness.

Table 1: Radiation Hardness Comparison

TECHNOLOGY	**TOTAL DOSE HARDNESS - Rads (Si)**
BIPOLAR:	
TTL/STTL	1×10^6
ECL	1×10^7
IIL	1×10^6
Linear	1×10^4
MOS:	
NMOS	7×10^2
CMOS (Bulk)	3×10^3
CMOS/RH	1×10^7
CMOS-SOS	1×10^6

Source: See Ref. 1.

NOTE: Achieving total dose hardness in CMOS-SOS is more difficult than in bulk CMOS, but SOS does appear to offer advantages relative to dose rate, with respect to SEE.

Silicon BIPOLAR technology is also heavily utilized in Linear devices, but analog devices require different transistor design characteristics from logic devices whose operation involves simple switching of logic states. Linear devices are affected by radiation in two ways.

(1) Low current transistor betas (current-gains) are degraded by surface effects similar to those which degrade MOS devices. Collector current (i.e. base current minus base - emitter leakage current times the beta of the transistor), is thus affected as a result of radiation exposure. When the leakage current (base-to-emitter) increases significantly as

a result of radiation, the transistor will not function properly at low current levels, causing problems with input impedance, input offset and open loop gains.

(2) Bipolar devices (Integrated Circuits) often contain parasitic MOS devices, which present no problem in logic devices. Bipolar logic circuits typically operate at 5V with logic thresholds below 2V also helps. The parasitics typically have turn-on voltages in excess of 30V. Bipolar linear devices, however, typically operate at higher voltages (with positive-to-negative supply differentials of from 30V to 40V, making them more susceptible to even small radiation induced shifts in the turn-on voltages of parasitics). The problem is partially solved by design layout changes.

Other processing characteristics such as the difference between silicon dioxide and silicon nitride (used for surface passivation) can also change the radiation tolerance characteristics of bipolar linear devices. With improvements in current technology, most such devices are rad-hard to one mega-Rad(si) level. One method to compensate for the transistor-to-transistor leakage current effects due to radiation is corrected by using dielectric isolation technique in bipolar devices.

Total Ionizing Dose (TID) Effects in CMOS Devices: CMOS-Bulk Devices (IC's) experience "latch up" due to a parasitic four-layer PNPN path, inherent in most unhardened devices. These parasitic four-layer devices act like a Silicon Control Rectifier (SCR), which once latched cannot be turned off without shutting off the power. Radiation hardening for total dose of such devices can be achieved by choice of technology and design changes to minimize the formation of such paths within an Integrated circuit. CMOS-SOS or CMOS-SOI devices do not have such paths and are inherently rad-hard up to one megaRad(Si), but are comparatively more expensive. CMOS-Bulk devices can be made rad-hard by introducing epitaxial layers to reduce the formation of PNPN paths, thus reducing the chances for latch up to one mega-Rad (Si).

Single Event Effects (SEE): High energy protons or heavy ions lose their energy mainly through ionization, i.e create electron-hole pairs as they traverse through p-n junctions or the depth of penetration in the semiconductor material. Some of the deposited charge recombines, and some is collected at the junction contacts. The net effect is a very short duration pulse of current that induces transient at internal circuit nodes. The magnitude of the charge , which is generally much larger for ions with high atomic numbers, depends on the energy and ion type, as well as the path length over which the charge is collected. The effect of these random charges on the circuit depends on a number of factors, including the minimum charge required to switch a digital circuit state, called SEU's. Single bit upsets are easy to correct by Error Correction Codes but multiple bit corrections may lead to problems, and can be corrected by redundancy, etc. Also, memory devices are hardened by design to minimize single event upsets. CMOS Static Random Access Memory (SRAM) cells can be hardened by adding capacitors, resistors, transistors or combination of these devices to the circuit, at the cost of circuit parameter degradation especially the speed.

If the CMOS-bulk process creates parasitic SCR's or PNPN structures, the excessive charge may cause a Latch up, leading to a SEL, which can sometimes lead to the destruction of the device. It

can be minimized by choice of rad-hard process or technologies. CMOS-SOS/CMOS-SOI, Bipolar and GaAs devices are not prone to latch up or SEL.

Latch-up in rad-hard devices is minimized through design and process using (a) numerous, regularly spaced well and substrate contacts in design, (b) thin-epi/shallow well CMOS processes, and (c) butting of the source-to-substrate and source-to-well contacts. The only certain way to eliminate latch up is to use CMOS-SOS or CMOS-SOI process that eliminates one of the parasitic transistors, thereby removing the possibility of latch up.

The problems resulting from SEL's are either immediate or latent damage which may reduce functional performance. Non rad-hard circuits or devices can incur damage from excessively high currents within a few microseconds. Once latch-up occurs, a device would remain in a high current, latched condition until power is turned off. Power cycling will be required each time latch up occurs, which will temporarily shutdown sections of the subsystem that share power supplies. Along with power cycling, circuits and subsystems affected by any component will have to be re-initialized.

Another potentially catastrophic SEE phenomenon called “Snapback” exhibits many of the characteristics of latch up and can occur in single MOS transistors structure. It can occur in SOS and SOI technologies that do not contain four-layer parasitic structures. A single high energy particle may trigger snapback if the field across the drain region is sufficiently high. Snapback is due to the prospect of a parasitic bipolar transistor existing between the drain and source region of a MOS transistor which amplifies avalanche current that results from the transversal of the heavy ion Cosmic ray particle. This results in a very high current between the drain and source region of the transistor, with subsequent localized heating.

Technical Rationale:

To ensure dependable and reliable electronic circuit designs, the radiation environment for Total Ionizing Dose (TID) and Single Event Effects (SEE) encountered at a specific height and orbital orientation during the space-craft mission must be determined. Such data is available from NASA documentation such as SSP 30512, "Space Station Ionizing Radiation Design Environment" and SSP 30513, "Space Station Program Natural Environment Effects Test and Analysis Techniques", applicable to the International Space Station Alpha. Goddard Space Flight Center documentation also provides this information.

All electronic devices/components will experience two radiation-related effects in space. The first, the TID effect is time dependent, and the second, SEE, depends on many factors and is independent of time. The two effects must be addressed separately in design, and as such, this guideline will define basic ground rules for selection of rad-hard devices (radiation tolerant up to a certain specified dose) which can tolerate the effects produced by space radiation, within specified safe limits.

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If the power is not turned off when latch up occurs in a power Metal Oxide Semiconductor Field Effect Transistor (MOSFET), the avalanche current within the parasitic SCR structure increases indefinitely to cause heating in the gate channel due to I^2R effect and leads to burn-out by a very high energy cosmic ray particle going through the transistor.

Another phenomenon associated with the power-MOSFET's is the gate-oxide damage called single-event-Gate-rupture due to the presence of an extremely large electric field, which causes a force on a trapped charge given by

$$F = q * E = q\frac{v}{d} \qquad \textbf{(1)}$$

where **q** is the presence of a charge trapped within oxide, **v** is the potential or voltage across the gate, and **d** is the thickness of the gate oxide. Both of the mechanisms are fatal to the power transistors.

Impact of Nonpractice:

Failures of components encountered in space due to the use of non-rad-hard devices can lead to catastrophic results, which may lead to loss of spacecraft and possibly loss of life. Disregard for these guidelines can cost a program significant resources and make the difference between success and failure of a space mission.

References:

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3. George C. Messenger, and Milton S. Ash, "The Effects of Radiation on Electronic Systems," Van Nostrand Reinhold Company, New York, NY, 1986